CLAIMS

What is Claimed is:

1. A system for processing digital signals comprising:

a signal conditioning filter comprising a first stage for mitigating degradations of a digital signal that occur according to a first time scale and a second stage for removing signal distortions that occur according to a second time scale, the second time scale being different than the first time scale; and

a signal integrity unit for controlling the signal conditioning filter by maximizing fidelity of the digital signals.

2. The system of Claim 1, wherein at least one of the first and second stage of the signal conditioning filter comprises a tapped-delay line filter.

3. The system of Claim 2, wherein the signal conditioning filter comprises a coefficient amplifier, the coefficient amplifier comprising a Gilbert cell multiplier.

4. The system of Claim 2, wherein the tapped delay-line filter comprises LC circuits.

5. The system of Claim 2, wherein delays are distributed across both the input and output branches of the tapped delay-line filter.

6. The system of Claim 2, wherein the parasitic capacitances from one of an input and output of the tap delay line filter are absorbed into the LC design circuit and used to implement the delay.

7. The system of Claim 1, wherein the digital signals comprise binary signals.

8. The system of Claim 1, wherein the digital signals comprise multilevel signals.

9. The system of Claim 1, wherein the first and second stages comprise various signal paths of different lengths where time delays produced by the paths are re-used.

10. A system for processing digital signals comprising:

a first filter stage operating according to a first time constant, for compensating for signal distortions that occur within a single symbol period and for integrating over less than a symbol period in order to substantially reduce at least one of ringing, jitter, and noise; and

a second filter stage operating according to a second time constant, the first time constant being smaller than the second time constant, the second filter stage for removing inter-symbol interference (ISI).

11. The system of Claim 10, wherein at least one of the first or second stage of the signal conditioning filter comprises a tapped delay-line filter.

12. The system of Claim 11, wherein the signal conditioning filter comprises a coefficient amplifier, the coefficient amplifier comprising a Gilbert cell multiplier.

13. The system of Claim 11, wherein the tapped delay-line filter comprises LC circuits.

14. The system of Claim 11, wherein delays are distributed across both the input and output branches of the tapped delay-line filter.

15. The system of Claim 11, wherein the parasitic capacitances from one of an input and output of the tap delay line filter are absorbed into the LC design circuit and used to implement the delay.

16. The system of Claim 11, wherein the digital signals comprise binary signals.

17. The system of Claim 11, wherein the digital signals comprise multilevel signals.

18. The system of Claim 11, wherein the first and second filtering stages form part of a unit for receiving digital signals.

19. The system of Claim 11, wherein the first and second filtering stages form part of a unit for transmitting digital signals.

20. A system for processing digital signals comprising:

a cascade of filters, where each filter comprises a variable gain amplifier connected between a first delay element and a second delay element, each filter equalizing a particular frequency band of a multilevel signal.

21. The system of Claim 20, wherein the variable gain amplifier comprises a Gilbert Cell multiplier.

22. The system of Claim 20, wherein the first and second delay elements comprise delay lines.

23. The system of Claim 20, wherein the first and second delay elements comprise delay lines that include LC circuits.

24. The system of Claim 20, further comprising a signal integrity unit for controlling each filter.

25. The system of Claim 22, wherein the signal integrity unit measures fidelity of the filtered signal, and gains of the variable gain coefficient amplifiers are controlled to maximize fidelity measured by the signal integrity unit.

26. A method for monitoring and improving the fidelity of a digital signal comprising:

receiving a digital signal;

applying an adjustable conditioning filter that compensates for signal distortions

determining a quality of the digital signal after the conditioning filter;

in response to determining the quality of the received signal, adjusting one or more parameters of the conditioning filter to improve the quality of the digital signal.

27. The method of Claim 26, wherein adjusting one or more parameters of the conditioning filter further comprises adjusting one or more variable gain amplifiers.

28. The method of Claim 26, further comprising propagating the received signal through a series of delay lines with each delay having approximately the same delay value.

29. The method of Claim 26, further comprising optimizing a quality of the digital signal by empirically calculating an estimated fidelity measure.

30. The method of Claim 29, wherein empirically calculating the estimated fidelity measure comprises using a coordinate descent.

31. The method of Claim 29, wherein empirically calculating the estimated fidelity measure comprises using a gradient descent.

32. The method of Claim 29, wherein calculating an estimated fidelity measure comprises determining a regularization component to guide a solution to the fidelity measure to a predetermined bias.